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# DIGITAL COMPUTER NEWSLETTER

**OFFICE OF NAVAL RESEARCH · MATHEMATICAL SCIENCES DIVISION**

The purpose of this newsletter is to provide a medium for the interchange among interested persons of information concerning recent developments in various digital computer projects. Distribution is limited to government agencies, contractors, and contributors.

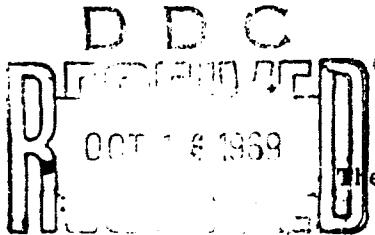
Vol. 12, No. 4

Gordon D. Goldstein, Editor

October 1960

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Approved by  
The Under Secretary of the Navy  
20 August 1957

This document has been reviewed  
for release and is approved for  
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Naval Exoskeleton Project

NAVEXOS P-645

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## COMPUTERS AND DATA PROCESSORS, NORTH AMERICA

### PENNSTAC - THE PENNSYLVANIA STATE UNIVERSITY - UNIVERSITY PARK, PENNSYLVANIA

In August 1960 the staff of the Computer Facilities, Electrical Engineering Department, The Pennsylvania State University, will install a new Read Out system in the Penn State Automatic Computer (PENNSTAC). This new Read Out system will present three major modifications. However, before discussing the new system it might be helpful to state the features of the old system.

The single operation code in the old system enabled the programmer to have information sent to the output device, a Flexowriter. A manually-positioned format switch controlled the number of digits to be read out. Carriage function information for the Flexowriter originated from a format tape placed in the Flexowriter reader.

As was stated before, three major modifications will be presented with the new system. First will be the Internal Output Control by means of which the output will be controlled almost entirely by the program. The format switch and the format tape will be eliminated. All carriage function information, as well as information on the number of digits to be read out, will originate from the program.

The second modification will be the addition of a second output device, a sixty-digit-per second Teletype Punch. The programmer will select as the output device either the Teletype Punch or the ten-digit-per second Flexowriter.

The third modification will be the incorporation of a feature which will enable the operator to read out one digit at a time by depressing a button. This feature will be valuable as an educational tool for teaching computer students the design methods involved in the solution of problems concerned with communication between the computer and an asynchronous device. Furthermore, the feature will be helpful during maintenance periods.

Editing of output information by the computer, impossible with the old system, will be permitted under the Internal Output Control. Furthermore, the increase in output speed - by a factor of six or seven - will make the computer more effective for many problems which are greatly output limited at the present time. Elimination of the format tape will allow the format to be changed without intervention. In addition, the one-digit control will provide a desirable educational and maintenance feature.

### NTDS - REMINGTON RAND - ST. PAUL, MINNESOTA

A new, extremely compact high-speed electronic computing system which collects, processes, and evaluates naval tactical data and recommends courses of action has been developed for the Navy by the Remington Rand Univac Military Division, St. Paul, Minnesota. The firm's role in the research and development phase of the program heretofore under strict security wraps, involved not only the initial feasibility study and the design and development of six computer prototypes, but also the development of at least 20 pieces of communicating peripheral equipment, each of which entailed design efforts as demanding as that required by the computer itself. The basic objective of the research and development phase was to determine the feasibility of automatic data processing for naval tactical situations. The computers and associated equipment - integrated with communications and sensor equipment - have undergone over a year of tests. These tests were designed to demonstrate the operational capability of the equipment.

Modular or building block construction contributes to the compactness and maintenance of the Univac Advanced Navy Computer. It contains 3,776 identically packaged electronic circuit modules. The entire Computer measures only 3 x 3 x 6 feet - less than the space occupied by

a businessman's desk. Rollout drawers permit easy and rapid access to the component packages. The computer is a general-purpose, stored-program machine with a very high-speed, random-access memory containing 1,000,000 bits of information. Access for a single word (30 bits) is 2.5 microseconds. The machine contains 64 instructions and can execute one in 20 microseconds.

New design concepts and the use of transistor-diode circuitry, rather than conventional vacuum tubes, are largely responsible for the computer's small physical size. Although it occupies only about nine square feet of floor space, the Univac Advanced Navy Computer does the work of two Univac 1103 computers, each of which occupies about 1400 square feet of floor space. Transistor-diode circuitry and new packaging techniques also minimize power consumption. The computer operates on 2500 watts of electricity.

As long ago as 1950, the operational control of huge naval task forces and ships had already become too complex for rapid handling solely by humans. Combat Information Centers (CIC's), consisting of small command groups aboard ships, served as shipboard or task force "Nerve Center." CIC's were mechanized to a degree by radars, teletype machines, radios, plotting boards, etc., but the Navy realized that a much greater degree of automation was vital in order to sufficiently increase its capabilities. Space age weaponry dictated an urgent need for automation and high-speed equipment in shipboard tactical systems. Swift advances in the field of electronics offered potent solutions to this problem. From a naval tactical standpoint, the use of computers for the collection, display, and dissemination of combat information permits the automation of many routine tasks, which can be performed indefinitely faster and more accurately, thus freeing men to concentrate on decision-making. The computer processes and correlates information obtained from such data-gathering sources as radar and sonar.

Computers aboard the units of a widely-deployed naval task force exchange information which, added to that held internally in its computer memory, provides complete knowledge of the overall tactical situation. All echelons of the command are given the facility to disseminate their orders automatically and at high speeds. This high-speed communication between computers enables all units in the task force to operate in an extremely well coordinated fashion... as though (the task force) were one huge ship. By simply inserting a new program, the computer can be made to handle new tasks and problems. Thus, the same computer can be used, regardless of the type of ship and its tactical responsibilities, and will be fully adaptable to future changes in tactical environments.

A tactical situation may involve an enemy who is widely dispersed, with many modern weapons (nuclear subs and warships, jet planes and missiles) at his disposal. The speed and saturation with which an enemy might launch an attack imposes an urgent need for the high-speed exchange of situation, decision and status information between task force units. Tactical situations develop rapidly and terminate quickly. Delays in reaction times peril the outcome of such an engagement. Modern weapons make the Navy's present-day combat direction problem harder than ever by imposing heavy tactical data loads on that function. The Naval Tactical Data System (NTDS) eliminates the data load by correlating all data into a clear picture of the tactical situation; processing data as required to aid the decision-making process; and communicating the action decisions to the selected weapons system. As weapon speeds increase, grease pencil or voice-telling techniques communicate the tactical picture too late for offensive and defensive action. Automatic, high-speed electronics equipment provides the commanders of forces and ships with a clear, concise picture of the tactical situation and alternative courses of action... in time to meet the enemy threat.

The Naval Tactical Data System represents a successful culmination of a joint cooperative effort between the Navy and Industry. Overall system's responsibility and operational concept and guidance have stemmed from the Office of the Chief of Naval Operations. The Bureau of Ships has been prime executor in System Technical Design contract administration and hardware implementation of the NTDS concept, aided in these duties by the Navy Electronics

Laboratory with respect to analysis test, evaluation, and design improvements of the experimental system. Major contractors, Remington Rand Univac, Hughes Aircraft Company, and Collins Radio Company, working in close cooperation, both with the Navy and each other, provided the important ingredient of industrial "know-how" necessary to translate the Navy's needs into fleet equipment.

#### WRUSS & GE-225 - WESTERN RESERVE UNIV. - CLEVELAND, OHIO

WRUSS. At present the Western Reserve University Relay Searching Selector (WRUSS) is being used as an information retrieval tool. All publications in metallurgy and allied subject fields are abstracted and encoded for machine searching (for a full description of methods, see J. W. Perry and A. Kent, "Tools for Machine Literature Searching," Interscience Publishers, Inc., New York, 1958). The abstracts are stored on punched paper tape, each identified by an abstract number. Questions in the field of metallurgy relating to specific or special interest with various boundary conditions are posed to the computer. As many as ten questions can be posed to the selector at any one time. The selector scans the telegraphic abstracts on punched paper tape and when it finds an abstract which satisfies the conditions posed to it in any of the questions, it prints the abstract number and the question numbers to which it relates.

GE-225. The delivery of the 8192 word core memory, GE-225 computer with additional features of the searching selector is scheduled for February 1961. The telegraphic abstracts for this computer would be stored on magnetic tape and searching will be much faster. Since the GE-225 will have capabilities of a high-speed computer which the WRUSS does not possess, the school is planning on building a computational center around the General Electric Computer. An educational program in data processing and computer applications will be initiated at Western Reserve University, and it will permit the various departments at the University to pursue their research utilizing the computer capabilities.

#### COMPUTING CENTERS

##### ANALYSIS AND COMPUTATION DIVISION - AIR FORCE MISSILE DEVELOPMENT CENTER - HOLLOMAN AFB, NEW MEXICO

Two Ampex FR 307 Tape Units have been added to the system. These units are able to handle IBM tape format and can be programmed by the computer to read, write, move, and rewind. Reading and writing can be performed in Binary or BCD mode. This setup makes the Univac Scientific computer, model 1103-A, completely compatible with IBM computers as far as magnetic tape is concerned and allows an interchange of information recorded on magnetic tape with IBM installations. For a description of the system see Digital Computer Newsletter July 1959, and April 1960.

##### COMPUTATION LABORATORY - NATIONAL BUREAU OF STANDARDS - WASHINGTON, D. C.

The capacity of the electronic computing facility, an IBM 704, was increased through the addition of a tape-controlled, high-speed printer. The computer remains on three-shift operation, performing computations arising in the work of the Bureau and, in addition, carrying the main computing load of several other Government agencies, and serving as a standby facility for the Weather Bureau.

Significant progress has been made on the automatic Russian-English translation scheme being developed by the Bureau for the Army Office of Ordnance Research. The Bureau project is characterized - in comparison with other projects concerned with machine translation - by emphasis on syntax in the conventional sense and by a system of predictions. A Russian word in a sentence "predicts" certain other grammatical forms, for example, a transitive verb predicts an accusative. The machine program first instructs the computer to transform the words of a Russian sentence into a highly condensed representation for matching in a glossary, then tells the computer to recognize the syntactical relations between the Russian words, and, finally, to put the corresponding English words into a meaningful sentence. Of these three facets of the Bureau's mechanical translation scheme, the computer program for the first and the main, or control, program for the second are now completed. In addition, significant progress has been made in the preparation and testing of the subroutines for handling the predictions.

#### HIGH ACCURACY RADAR DATA TRANSMISSION SYSTEM - PACIFIC MISSILE RANGE - POINT MUGU, CALIFORNIA

A High Accuracy Data Transmission System, using voice facilities as the transmission medium, will soon become operational at the Pacific Missile Range. This system connects transmitting sites located at Point Magu, Point Arguello, Vandenberg, and San Nicholas Island with IBM 709 Data Processing Systems located at Point Mugu and Point Arguello. The system provides the capability of transmitting data from one to six instrumentation sites, to two 709 computing facilities as a test is in progress. The data can immediately be processed by either or both computers to meet the computational requirements of the test. In addition to transmitting the data to the computers, magnetic tape recordings are made at each transmitting site.

The transmit terminal utilizes a DH-10 Data Distribution Unit (DDU) and a modified TE206 Kineplex Transmitter. The DDU utilizes PMR range time to interrogate all instrument sites synchronously. Kineplex transmitter clock data insures that the output of the DDU will be in synchronism with the Kineplex Transmitter. Range time, redundancy data, instrumentation site identification information, and data quality are combined with the sampled digital data from the instrumentation sites. This data is placed in the required format for transmission and recording. The DDU is capable of interrogating the instrumentation system at 10, 20, or 40 samples per second. However, the transmission system has a maximum transmission capability of 20 samples per second. With a sampling rate of 40 samples per second, every other sample is sent over the transmission system and every sample is recorded at the transmitting site. The tape recorded at the transmitting site may be utilized for post-flight data processing. The TE206 Kineplex Transmitter converts the digital data into phase-shifted audio tones. These audio tones may be transmitted over a standard voice facility (telephone line or microwave) of an indefinite length. The Kineplex link has a transmission capability of 2400 bits per second.

The receive terminal utilizes six modified TE206 Kineplex Receivers and a DH-14 Data Multiplex Synchronizer Unit (DMS). The TE206 Kineplex Receiver accepts the phase-shifted audio tones from a remote Kineplex Transmitter and converts the tones back to their original digital form. Each receiver is connected to a selected transmitter at a remote site and there is a maximum of six independent data sources for the DMS. These sources are synchronous to the Kineplex Transmitter which in turn is synchronous to the DDU and PMR range time.

The Data Multiplex Synchronizer Unit (DMS) accepts the binary data from the Kineplex Receivers. The DMS assembles the data into a 24-bit broadside format for entry into the 709 computer. Longitudinal parity is checked and in the event of bad parity, a mark is presented to the computer along with the data. When controls between the DMS and computer have been established, the data is multiplexed into the computer core memory unit. A signal is then sent to the computer to indicate that the data has been transmitted to core storage. This

process is repeated until completion of the test.

#### COMPUTATION CENTER - U. S. NAVAL WEAPONS LABORATORY - DAHLGREN, VIRGINIA

High-Speed Printer for 7090. Installation of an IBM 7090 system, which will share the workload with the NORC, was begun in August of this year. To supplement the output facilities of the 7090, a Charactron printer/plotter is being constructed by the Computation Center staff. The printer/plotter will be similar to the one now attached to NORC, except that the new device can operate either on-line (via a tape channel) or off-line from magnetic tape. Maximum speeds will be 16,000 characters or 10,000 plotted points per second. Two 35 mm cameras will be provided, one of which includes processing and display of a recorded page within eight seconds after recording.

New NORC Memory Performance. Some statistics now available indicate the excellent performance of the 20,000 word core memory installed in the NORC earlier this year:

|       | <u>Scheduled Computing Time</u> | <u>Down Time Due to Memory</u> | <u>Memory Error Stops</u> |
|-------|---------------------------------|--------------------------------|---------------------------|
| April | 633 hrs.                        | 2.2 hrs.                       | 18                        |
| May   | 643                             | 1.7                            | 6                         |
| June  | 609                             | 5.2*                           | 7                         |
| July  | 637                             | 0.1                            | 2                         |

\*3.5 hours lost through accidental shorting of terminals with oscilloscope probe; transistors in 23 packages were destroyed.

#### COMPUTERS AND CENTERS, OVERSEAS

##### ATLAS - FERRANTI LTD. - MANCHESTER & LONDON, ENGLAND

ATLAS is the latest computer to be announced by Ferranti Ltd., and, like the earlier Ferranti Mark I and Mercury Computers, it is the result of collaboration between the Company and a team at the University of Manchester headed by Professor T. Kilburn. Atlas is a very fast parallel computer, employing solid state techniques exclusively, having, it is claimed, the highest computer speed obtainable at reasonable cost - meaning that to obtain an even faster system would involve a disproportionately large increase in electronic equipment.

ATLAS incorporates several technical advances: a fast carry adder in which addition of two numbers from the associated registers takes approximately 0.3 microseconds; a fixed store with an access time of 0.3 microsecond; and a two-core per bit ferrite store with a cycle time of 2 microseconds. In addition to enabling the computer to perform large-scale computations efficiently, the high speed has been used to simplify the control of input/output equipment by allowing the central computer to deal with their organisation, and the data transfers on an interrupt basis by means of programs held in the fixed store. The design of the system also incorporates an entirely new and sweeping approach to the problem of store utilization. The result is a flexible and economical system that can be applied with equal efficiency to large scientific calculations and to commercial data-processing work.

A prototype version, proving the techniques involved, is currently under test at Manchester and the first production machine for Manchester University is scheduled for completion by the end of 1961.

Operating Speeds. Because of the possible overlapping of instructions it is impossible to give exact times for obeying individual instructions. However, the average time for an addition (of either two 48-bit floating point numbers or two 40-bit fixed point numbers) is expected to be 1.1 microseconds, and the time for multiplication is such that, for example, the summing of a polynomial will take from 5 to 7 microseconds per term.

Instruction Code. An instruction occupies a full word of 48 bits; with 10 bits for the function, 7 bits for each of two index addresses (named B-registers in Manchester tradition) and 24 bits for a single main store address. This generous allowance of instruction bits will cater for any developments of the system that may occur later. At present over 300 different functional instructions are available to the programmer. About one third of these, covering the common floating and fixed point arithmetic operations, and logical and "red-tape" operations are "basic" instructions which are directly engineered in the hardware, while the remainder are concerned with a system known as "Extracode". Extracode instructions cover a wide range of more sophisticated operations (for example, double precision arithmetical operations); provide for the evaluation of functions (sine, cosine, etc.); and organise peripheral operations and data handling. To the user the two types of instruction are indistinguishable, but with an extracode instruction the function bits are used to determine an entry point to a subroutine of basic instructions held in the fixed store, the remainder of the instruction being available for parameters. When this subroutine has been obeyed control returns automatically to the instruction following the initiating instruction. The extracode facility makes available to the programmer a far wider range of instructions than would otherwise be possible without undue complication (and hence slowing down of the basic instructions). The high speed of operation of the fixed store enables many simple subroutines to be executed in times not much greater than those for basic instructions.

Two independent computing units exist within. The central accumulator is equipped to deal with arithmetic operations both on 48-bit floating point numbers (8-bit octal exponent with 40-bit signed mantissa), and on 40-bit fixed point numbers. In addition there is a mill associated with the index registers in which 24-bit logical and test operations can be performed. Instructions may proceed within these two units simultaneously.

Storage. The high speed makes it a suitable computer for efficient solution of problems demanding a large internal store, and therefore 24 bits have been allocated to the address part of instructions. Virtually unlimited core storage can be added in modules of 4096 words. Each section of 4096 words has its own independent access system so that, with several sections, a mean access rate of over a megacycle is achieved.

The 24 address bits in an instruction are allocated in the following way. The first bit separates the store into two parts: the first a "private" part comprising the fixed store and a special section of core store used by it as working space, and registers associated with input/output equipment; the second is the main store available to all programs. The last three bits of an address are reserved for specifying 6-bit characters within a 48-bit word so that instructions may refer to 48-bit words, 24-bit half words or 8-bit characters. The remaining 20 bits enable up to approximately one million words to be included in the main store.

The fixed store is constructed (in modules of 4096 words) from a woven wire mesh into which ferrite slugs are inserted, the pattern of rods corresponding to the pattern of bits to be stored. The access time for this store is 0.3 microseconds.

Organization of Storage Allocation and Time Sharing. The organization of the main store is the most revolutionary feature of the machine. The store is regarded as being comprised of blocks each of 512 words, so that 9 bits of the address determine the position of a word within a block and 11 bits identify the block. However, these 11 bits do not define directly the physical position of the block; instead each block of information is identified by an 11-bit floating label independently of its actual position in the store. With each physical block (or "page") in the

core store there is associated a "page-address register" holding the label of the information block that currently occupies that page. Before every store access these registers are consulted simultaneously and very rapidly and their contents are compared with the block address required. The position bits are then used to determine the particular word to be extracted from the page whose page-address register agreed with the interrogating block address. Special equipment is supplied to ensure that this process does not limit the rate of transfers to or from the store. Information held in magnetic drums (if any) is also addressed in a similar way, a directory of all block labels being held in the working store associated with the fixed store.

This indirect method of addressing provides a simple basis for the complete automation of the allocation of store space to several programs to be run on a time-sharing basis and also enables the integration of core store and magnetic drums into what may be regarded by the programmer as a one-level store.

An object program having priority can proceed at top speed only when its currently required instructions and data are in the core store. However, a program may, at some stage, make reference to a word in a block not in the core store. In this case no agreement would be found when the page-address registers are interrogated, and this leads to an automatic interruption of the object program, control being transferred to a special routine held in the fixed store. This routine has access to the directory of block labels and so can organise appropriate transfers of information between the core store and the drum store so that the object program may proceed. This routine will, of course, update the page-address registers and the block directory. By associating with each page-address register a "use bit", it is intended to keep a record of the relative frequencies of references to the pages of the core store. The routine uses this information when deciding which blocks to leave in the core store, in order to minimise the number of transfers needed. Although it is expected that most programs will make use of the automatic drum transfer system, a programmer may, if he prefers, organise drum transfers in the more conventional way.

Further program features assist in organizing the time sharing of object programs. The block directory is extended so that an appropriate program number is stored with each label. A directory is kept of the activities of all input/output equipments. In addition, the page-address registers are extended by one bit, a "lock-out bit", ensuring that access can never be made to pages not associated with the currently running program. By making use of these directories and updating them as necessary the fixed store routine can administer the whole process of store allocation for all programs in the machine. The only store protection that need be provided by hardware is to prevent object programs fouling the directories. This is simply done by restricting reference to the "private part" of the store to programs held in the fixed store.

Index Registers. The control registers, accumulator exponents, and a few special purpose registers are included among the 128 B-registers. These are flip-flop registers while the remainder are assembled in a ferrite core store with a cycle time of 0.5 microseconds. For instructions using the accumulator both B-addresses may specify independent 24-bit modifiers, while with most other instructions one B-address specifies a 24-bit operand and the other a modifier for the main store address.

Input/Output Equipments. A large range of standard input/output equipments including magnetic tape mechanisms (90,000 character transfer rate), paper tape and card readers and punches, line printers, graphical displays, etc. Magnetic tape (and also drum) transfers of 512-word blocks are autonomous using core store cycles as required. Single character or word buffers are associated with other units, the unit signalling when the buffer requires attention so that an appropriate fixed store routine can be entered on an interrupt basis to deal with the assembly of blocks of data.

Size of Installation. Currently the design envisages a core store of 16,384 words as a minimum, extendable by units of 4096 words; a fixed store of 8192 words minimum again extendable by 4096 word sections; up to 16 magnetic drums each holding 24,576 words; up to 32 tape mechanisms communicating via 8 independent channels; up to 8 line printers and virtually unlimited other peripheral units.

#### HITACHI COMPUTERS - HITACHI, LTD. - TOKYO, JAPAN

Hitachi Co. Ltd., manufactures many digital computer models for use in the scientific and business fields. Some are also in use for seat reservations of trains and aeroplanes. Representative types are HIPAC-101, HIPAC-103, HITAC-102, HITAC-301, and HITAC-502. The name HIPAC is the abbreviation of Hitachi Parametron Automatic Computer while HITAC stands for Hitachi Transistor Automatic Computer.

HIPAC-101 is the modified production model of the HIPAC-1 (See DCN April 1959) which was exhibited at the UNESCO June 1959 in Paris. HIPAC-101 using the Japanese invented parametrons for its logical element, is a very reliable computer. HIPAC-103 is more versatile and is capable of high speed calculations. HITAC-102 uses transistors as logical elements; models are in operation at the Japan Electrical Technical Laboratory and other laboratories. HITAC-301 is used as an EDPM system for management. This computer is designed for use with IBM card input-output devices, and is expected to be in extensive use in the near future. HITAC-502 is a computer for control. See table on page 9 for additional features of machines.

#### LEO III - LEO COMPUTERS LTD. - LONDON, ENGLAND

LEO Computers Ltd., of Queenway, London, England, recently announced a new transistorised data-processing system of advanced design known as LEO III to be available from mid 1961. The prototype is now being assembled and tested, and commitments for three systems have already been accepted.

LEO III is a fast parallel system based on a binary arithmetic unit of 40 bits plus sign bit, which is adapted to carry out arithmetic directly in any system of units including the decimal, but equally quickly and easily in any mixed radix system such as sterlings, weights and measures, coinage, etc. The radix conversions normally associated with binary computers are thus avoided. Fixed point addition takes 40 to 50 microseconds and fixed point multiplication from 300 microseconds. Optional floating point facilities are also available.

Access to the store, which comes in units of up to 4096 words each, is time-shared on a priority system to allow input/output transfers to be interleaved with computing. This form of time-sharing is performed automatically and without reference to the programme, under control of a "Store Access Control"; up to 4 units of storage, i. e., 16,384 words can be controlled by one Store Access Control unit. Another Store Access Control unit can be added if desired bringing the total storage available to 32,768 words. All stored information is checked by means of two parity bits. Two sign bits may be held with each long word, enabling two short numbers to be held together. The word length in store is, therefore, 44 bits. At present the store cycle is 15 microseconds.

A comprehensive single address instruction code is used with flexible facilities for address modification (indexing), giving effectively the same number of modifier registers as there are storage locations. An instruction is represented by 21 bits so that a 4096 word store holds 8192 instructions. Special instructions are provided for packing and unpacking data from input/output transfers, for floating point working, for sorting, for effectively exchanging the information between two designated storage areas, and for recording a block of data magnetic tape from a series of separate storage areas. The provision of these facilities is made easier by making extensive use of microprogramming, the conception of which was originally due to Dr. M. V. Wilkes of the University Mathematical Laboratory, Cambridge, England. In LEO III a separate core matrix is used for every action, or group of related actions, so that additions can readily be made after the machine is built and without great delay or expense.

Provision is made for operation of several programmes held in store at the same time using the interrupt mode. Interruptions are dealt with in accordance with priorities written into the programme itself so that priorities may be readily revised to suit new circumstances. This form of time-sharing is entirely distinct from the automatic sharing of access to store which is not linked with the interrupt facility in any way. Interruption can be used to ensure

| Type                             | HIPAC-101  | HIPAC-102   | HIPAC-103  | HIPAC-301   | HITAC-502  |
|----------------------------------|--|---|--|---|--|
| Purpose                          | Scientific   | Scientific  | Scientific   | Business  | Control  |
| Main Drum Capacity               | 2048 words   | 4000+200=4200   | 8192   | 2200  | 8000   |
| Core Memory Capacity             | -  | 50 words  | 1024 to 4096   | 200   | 192  |
| Access Time                      | 5 milliseconds   | 5 ms<br>1.25 ms (Quick)   | 40 $\mu$ s   | 3 ms  | 7.5 ms   |
| Auxiliary Drum Capacity          | -  | 8000 words<br>(max. 10)   | -  | 8000 words<br>(max. 10)   | 120 $\mu$ s (core)   |
| Arithmetic Mode                  | Binary   | Decimal   | Binary   | Decimal   | Binary   |
| Floating Point                   | Programmed   | Built-in  | Built-in   | Programmed  | Programmed   |
| Word Length                      | Sign + 41 bits   | S + 11 digits   | S + 47 bits  | S + 12 digits   | S + 23 bits  |
| Operating Speed                  | Quick<br>(incl. access time)                                   | 5.5 ms<br>Multiplying 7.5 ms<br>Dividing 23.0 ms  | 5.5 ms (1.75 ms)<br>10.8 ms (7.05 ms)<br>6.0 ms (6.0 ms)                               | 0.4 ms<br>1.8 ms<br>6.5 ms  | 3.3 ms<br>9.8 ms<br>9.8 ms   |
| Instruction Type                 | 1-1/2 address<br>(two instructions)<br>(per word)              | 1-1/2 address   | 1-1/2 address  | 1-1/2 address<br>(two instructions)<br>(per word)   | 1-1/2 address<br>(two instructions)<br>(per word)                                      |
| Vocabulary Of Basic Instructions | 62   | 122   | about 100  | 98  | 60   |
| Index Register                   | 2  | 3   | 3  | 2   | 2  |
| Optional Accessories             | Flexowriter<br>Photo Tape Reader                               | Flexowriter<br>Photo Tape Reader<br>Line Printer<br>Auxiliary MD Unit<br>Mag Tape Unit<br>High-speed tape punch | Flexowriter<br>Photo Tape Reader<br>Line Printer<br>Auxiliary MD Unit<br>Mag Tape Unit | Flexowriter<br>Photo Tape Reader<br>Line Printer<br>Auxiliary MD Unit<br>Mag Tape Unit<br>Card Read punch | Flexowriter<br>Photo Tape Reader<br>Line Printer<br>Auxiliary MD Unit<br>Mag Tape Unit |
| Electronics                      | Parametrons 5,500<br>Transistors 600<br>Tubes 50<br>Diodes 400 | Transistors 6,000<br>Diodes 40,000<br>Transistors 1,500<br>Diodes 2,000   | Parametrons 6,000<br>Transistors 35,000<br>Diodes 35,000                               | Transistors 6,000<br>Diodes 35,000  | Transistors 1,500<br>Diodes 10,000   |
| Delivery Time                    | 6 Months   | 6 Months  | 8 Months   | 8 Months  | 5 Months   |

that the fullest possible use is made of the available input/output machinery, by assigning certain units for one job and the remainder for a different job.

All input/output devices are linked to the Store Access Control by means of suitable electronic control circuits designed to convert information between the form appropriate to the record medium (paper tape, cards, magnetic tape, printed form etc.) and that used in the store. These control circuits are built in separate cabinets and are known as "assemblers". Due to the use of time-shared store access, buffer storage in the assemblers themselves can be restricted to one or two words. Areas of the mains store are assigned by programme for use as buffers and may, therefore, be exactly the size required for any particular job.

Input and output media include paper tape, cards, and magnetic tape; in addition, fast and medium speed printers may be attached. Paper tape is read at 1000 characters per second, cards at 400 or 600 per minute, and magnetic tape at 45,000 characters per second on 1/2" tape or 90,000 characters on 1" tape. Output speeds are 100 characters per second on paper tape, and 100 or 250 cards per minute; up to 850 lines per minute can be printed with the fast printer. Comprehensive checking facilities are included, verifying the actual reading and recording processes as well as the transfers from store to the peripheral control units ("assembler").

The transistorised circuits are mounted in individual cabinets linked by cables each fitted with its own ventilation and stabilised power supplies, thus facilitating installation and subsequent rearrangement or extension of the system. As a result of this form of construction it is possible to link together the assemblers for say magnetic tape and the high-speed printer giving a powerful off-time printing unit. Alternatively the transfers between tape and printer can be made by the computer itself on an interrupt basis which still leaves more than 90% of the time free for other jobs. The greatest care in circuit design has been taken to secure the widest possible operating margin and fullest interchangeability of packages. All circuits are designed to function correctly over an ambient temperature range of 10 to 40°C.

#### NEW COMPUTING CENTER - UNIVERSITY OF MILAN - MILAN, ITALY

The University of Milan Computing Center was established at the end of 1959. The Center will be equipped with the digital or analog computing devices that will be regarded as useful for the development of the activities of the Center. At the present time, the Center covers an area of about 160 square meters, including air conditioning and maintenance areas. The Computing Center is primarily intended as: (a) A teaching facility for the training of students, largely within the Mathematical Department in the field of numerical methods, programming, and data processing. (b) A no-charge computing facility for the University of Milan departments of Mathematics, Physics, Chemistry, Biology, Medicine, and Economics. (c) A means for the development of scientific and technical cooperation between University of Milan and industrial organizations or external scientific laboratories.

The Center is sponsored by a Scientific Committee, that is made up of university professors and industrial experts in the field of computers, data processing, or numerical methods. Operation of the Center is under the control of a Director. As soon as possible the Center will employ a small permanent staff consisting of 3 to 4 programmers, 1 consolist, and 2 operators for the punched card equipment. The use of the Center's equipment will be on an open shop basis; users training courses will be organized periodically to explain the programs and machines of the Center.

As a result of a special agreement between University and Remington Rand, Italy, the Center is equipped with a Univac Solid State Computer (U.S.S.90) using as input-output 90 column Remington Rand cards. The U.S.S.90 is a magnetic drum solid state computer (drum runs at 18000 r.p.m.) with 5000 memory positions, each of ten decimal digits plus sign, connected on-line with: a high-speed printer (600 lines p.m.), a high-speed reader (450 cards p.m.), a read punch unit (150 cards p.m.). The basic time is 17 microseconds; operating speeds (included minimum access-time to memory) are as follows: Compare, transfers, and other logical operations 51-68 microseconds, Sum and subtraction 85 microseconds, Multiply and divide times range from 200 to 2000 microseconds.

CHARACTER RECOGNITION - SOLARTRON ELECTRONIC GROUP LTD. -  
FARNBOROUGH, ENGLAND

Solartron has recently received two additional contracts for their reading machine. The first is from Domestic Electric Rentals Ltd., who have a chain of shops renting television sets. They are installing National Cash Registers in all their branches, and using these machines the cashiers will be able to record the account number of each customer, together with his payment. The audit rolls from each of these machines will be returned to Head Office each day where the information will be processed by the Solartron reader, the output of which will operate an I. C. T. gang punch to produce 80 column cards. These cards will then be processed in a standard punched card installation.

The second order is from Montague Burtons Ltd.; this firm has a chain of shops selling mens clothes on credit. Each customer is issued a credit card on which can be recorded each payment made and which has attached to it an embossed plate bearing the account number of the customer. When the customer makes a payment this card is presented, and is used to print the account number on a roll of paper within a point of sale printer. The amount paid is set up on keys and recorded alongside the account number. The advantage of using an embossed plate for the account number, is that it avoids any error of entry. The output from the reader will operate an I. C. T. gang punch to produce 80 column cards which will be processed in a computer installation.

SEL-K 10 TAPE UNIT - STANDARD ELEKTRIK LORENZ -  
STUTTGART, GERMANY

The Informatik Division of Standard Elektrik Lorenz AG (an ITT associate located in Stuttgart, Germany) has announced the development of a new magnetic tape transport designated as the SEL-K 10. This new type of a large-file memory is designed to combine the unlimited recording capacities of standard magnetic tape units with the speed advantages of the rapid-but-expensive random access stores, thereby making this unit especially suitable for commercial data processing assignments.

The unit consists of 10 independent magazines, each magazine having its own magnetic read/write head and a maximum length of 100 meters of tape. One shaft provides the drive for all 10 magazines in the unit. A return-to-zero device automatically brings the tape back to its middle point when a magazine is in "Rest-Operation".

Up to nine K-10 units can be attached to a maximum of 4 control units via an electromagnetic crossbar switch arrangement. This results in the possibility of obtaining simultaneous access to 4 out of a maximum of 90 tapes, with each tape having a speed of 2.5 meters per second.

The SEL-K 10 construction is precise and sturdy but retains characteristics of compactness and simplification to allow for attractive market pricing in Europe as well as in America. Additional information can be obtained from Intelex Systems Inc., 67 Broad Street, New York 4, New York.

TR 4 - TELEFUNKEN - BACKNANG/WÜRTT., GERMANY

The Telefunken Digital Computer TR 4 features short access time to the high capacity working stores, high running speed of the magnetic tapes, together with the wide range of simultaneous operations of several units within the system to match the high processing speed of the computer. The comprehensive list of instructions may at option be supplemented to give the machine maximum versatility for many special applications. The computer system consists of 4 main components: Arithmetic Unit, Storage Unit, Control Unit, and Input-Output Unit. All four units may operate independently and are combined by means of the distributor register (DR). Thus real simultaneous operation is achieved.

The word length in both the arithmetic and the control units is 48 bits. Numbers have 47 numerical binary digits and 1 tag bit. This tag serves to subdivide the stored numbers into groups, following the requirements of the program; e.g. a matrix may be broken into lines or columns. The tag is used, among other applications, in instructions where the address calls for a whole group of cells rather than a single word. The last cell of a group will then be tagged. The coefficients of a polynomial, for instance, form a group. The instruction "polynomial evaluation" will cause the polynomial value to be computed in the arithmetic unit. Another example is the scalar product which is used to multiply the line of one matrix by the column of another matrix. Fixed Point Numbers are 48-bit positive or negative binary numbers. These binary digits correspond to the accuracy of 13 decimal positions, or they represent positive or negative decimal 11-digit numbers, with figures in direct binary code. Floating Point Numbers contain a 38-bit mantissa plus sign and an 8-bit exponent. The exponent indicates the position of the point which is automatically shifted during the process of computation in such a manner that as many significant digits as possible are carried on in the arithmetic process while leading zeros are dropped. The capacity thus obtained without causing an overflow ranges from  $2^{-508}$  to  $2^{+508}$ , i.e. from  $10^{-152}$  to  $10^{+152}$ , at a 38-bit accuracy, or a 11-figure decimal accuracy, respectively.

Instruction Words comprise two orders of 24 bits each. Each order consists of an 8-bit operational part and a 16-bit address section. Generally these two portions are completely coded, hence the orders may be referred to as genuine one-address-instructions in the true sense of the word. Modification of an address with an index is performed by a preceding modifier instruction. Alpha Words generally comprise 8 alpha-numeric characters of 6 bits each. This is the way, for instance, the machine accepts a program written in alphabetic and decimal expressions, without restriction to a fixed word length, and converts it into binary representation. Any other subdivision of these 48 bits into groups of individual meaning may, of course, be used in programming.

The Word Length in the memory is 52 bits. In addition to the 48 binary positions already mentioned, there are: 2 check positions for automatic check of computation and transfer, which are not being affected by the program in any way (modulus three check); and 2 positions for type identification, by which four different types of words (see above) are identified for conversion purposes, and other applications.

The Arithmetic Unit is capable of performing the usual arithmetic and logical operations in fixed and floating point notation. It may execute accumulative multiplications, extract the square root and combine portions of different words to form new words. Furthermore, additions can be done directly into the memory. The arithmetic unit is composed of 5 registers which are in practically direct connection with the memory: The multiplicand register (MD) holds one operand of an arithmetic operation. The accumulator (AC) is the register capable of performing arithmetic operations. The multiplier quotient register (MQ) acts as counting register in the multiplication and division processes and may serve, if required, as a lower extension of the accumulator. The carry register (CR) is of importance for the internal operation of the machine. It stores the carry, thus allowing very quick multiplication. The logical "and" combination is formed in the carry register. The auxiliary register (AR) serves as a high-speed memory cell. It enables the arithmetic unit to perform, for instance, accumulative multiplications and thus to evaluate the scalar product.

The high computing speed results from the combination of parallel register operation and the high clock frequency of the Telefunken uhf transistors. The registers consist of static flip-flops with capacitor pre-stores ("register elements"). The technique of the switching network used for combining and control purposes is such that a two-stage operation is carried out with passive circuit elements. The first stage comprises and-circuits, whereas the second stage incorporates the or-circuits. The register elements for one binary position and the diode network interconnecting them are mounted on a printed circuit board in the arithmetic unit.

Operating Speed, binary (decimal), without access, Average figures:

|                | Fixed Point         | Floating Point |
|----------------|---------------------|----------------|
| Addition       | 5 (13) microseconds | 16             |
| Multiplication | 30 (500)            | 30             |
| Division       | 105 (500)           | 90             |

The Storage Unit consist mainly of quick access (write memories). The basic equipment contains Two Working Stores (St) with a capacity of  $2^{12} = 4096$  words each, with a word length of 52 bits. They are in simultaneous operation, independently from each other, with a cycle rate of 6 microseconds (access time 2 microseconds). Provision has been made for the extension of one of the stores to a maximum capacity of 28,672 words. The Permanent Store (PS) holds informations which may be read out but cannot be modified by the program. Its capacity is  $2^{10} = 1024$  words for standard programs such as input-output routines (conversion), check routines or frequently required functions. Extension of the store to a maximum capacity of 4096 words is possible. The Index Store (IS) serves for the storage of addresses. The word length, therefore, is 16 bits, with a total capacity of  $2^8 = 256$  words. The index store, too, operates simultaneously with the aggregates of the working store. It accepts, for instance, indices for modification and substitution of addresses, and loop counting, as well as the return addresses for subroutines. The initial and the final values as well as the pace length of a loop index can be held either in the working store, the index store or in the program instructions, alternatively. The privileged control of input-output give the index store a further special specification. The Control Unit controls the various units of the computer and their interconnection, and consists of following 3 registers: The Program Register (PR) accommodates 1 word, i. e., 2 instructions; The Control Counter (CC) indicates the cell from which the next instruction is to be retrieved (in case of subroutine jumps, its contents will be kept in the index store); and the Index Adder (IA) may take over an address from the index store and add it to the address of the instruction to be executed. The sequence of operations is directed by the micro-program control unit (MC). Instructions are formed here out of individual "micro-operations" in the same manner as a program is made up from various individual instructions. The only difference is that the execution of a micro-operation always requires exactly one cycle (0.5 microseconds), and that various micro-operations may be carried out simultaneously. Micro-operations are, for instance, transfers between the individual registers, elementary shifts, and elementary combinations. They may, like instructions, be executed conditionally; jumps and loop counts do occur here also. The micro-programs are wired on plug-in boards which are easily removable. Almost 250 instructions are available and may be even supplemented by some more, if desirable, in order to keep up with the customer's special requirements and wishes. The Input-Output Unit is an interconnection device between the fast computer and equipment of lower operating speed. To this end, the unit makes use of 5 Input-Output Register (IO) which may all operate at the same time and independently from one another. Each of them is capable of holding one complete word and has a channel of its own for parallel transfer to the distributor. Up to 8 equipments of different operating speeds may be linked to each of the four IO registers. The 5th IO register is reserved for the connection of the monitoring typewriter at the control panel. The Control Device assigned to the above registers automatically performs their loading or unloading, i. e., it may convert parallel words into serial words with parallel characters and vice versa and buffer between the various operating speeds. The information read from the magnetic tapes is automatically checked in the IO register. The code used on the tapes contains additional test information produced automatically in the input-output register. As soon as an input-output register has been loaded or unloaded, resp., the control device releases a message, interrupting the running program and effecting parallel transfer of one word between the input-output register and the working store. Transfer of whole information blocks between input-output units and working stores is thus controlled independently from the program. The addresses required for this purpose are stored in the index store. The program only needs to start the magnetic tape to set this block control in operation.

For input-output magnetic tape units, punched card and punched tape equipment, high-speed printers and, if need be, analog/digital and digital/analog converters are used. Off-line card/tape converters are in preparation.

Special magnetic tape units are being designed for a tape speed of 8 ft/sec. Their transfer rate is 37,500 char/sec. The tape is 1/2" wide. Information is stored on 6 tracks while a 7th track records one check pulse per character (parity check). The 8th track is the timing track. A further character per word added automatically allows error correction or error identification. On magnetization, the recorded information is checked via the read-head, by verifying its parity. The magnetic tape unit employs tape reels of international use (10, 5"), holding a tape with a minimum length of 2300 ft. Information on the tape is arranged in blocks of arbitrary length. These are separated by gaps. The tape will in general be stopped automatically as soon as a gap is read, or if during the recording process no further information is received from the computer for a certain period. The command "Start", specifying the IO register together with the magnetic tape unit connected to it, will cause the tape in question to start moving and will prescribe the travelling direction and the mode of operation (reading is possible in either direction). The order is executed regardless whether tapes connected with other IO registers are being processed.

High-Speed Printers may preferably be operated independently from the computer by magnetic tape units. Tape errors are corrected or faulty lines are marked. If a high-speed printer of the Anelex type 56/160 is employed, 15 to 20 lines (72, 120, or 160 characters per line) are printed per second.

Card-to-Tape, and Tape-to-Card Converters are planned. The computer itself, however, may, due to the facilities of internal parallel operation, read punched cards or tapes and convert them to magnetic tapes or vice versa, while another program is being processed. Thus, the computer is serving as a card/tape or tape/card converter.

## COMPONENTS

### PHOTOCROMIC PROJECTION DISPLAY - NATIONAL CASH REGISTER COMPANY - HAWTHORNE, CALIFORNIA

A new concept for dynamic plotting of real-time situations was unveiled by the National Cash Register Company. The novel photochromic display system uses NCR developed photochromic dyes which can be changed reversibly between two distinct color states. The dyes are coated on transparent slides forming part of an optical projection system. The color of the dyes is altered in chosen areas by special light sources to create the real-time plot of data being processed by electronic systems. This small-scale picture is projected onto a large wall or other suitable viewing surface so that the data can be viewed at the instant of writing. By insertion of tiny masks in front of the writing light source, the system can project any symbol from a dot, to a letter or other complex shape.

The color changes are reversible in response to specified wavelengths of illumination, and the persistence can be controlled from a fraction of a second to hours. Multiple real-time plots can be written simultaneously on the same slide and projected through a single lens system. Background maps or reference material may be inserted and changed rapidly. Provision can also be made for selective or total erasure of plotted information. Two of the outstanding characteristics of the photochromic technique are its inherent ruggedness and small size.

Applications of the unit include plotting of missile paths or satellite orbits, presentation of weather information, and aircraft traffic control situations. The display is one of several projects currently underway at the Electronics Division for military applications. Others include megacycle memories made from the NCR magnetic rod and a militarized ferrite core memory packaged for shipboard systems.

**ALL-MAGNETIC ARITHMETIC UNIT - STANFORD RESEARCH INSTITUTE -  
MENLO PARK, CALIFORNIA**

An arithmetic unit employing only ferrite elements and wire has been designed and constructed at Stanford Research Institute under the sponsorship of the Computer and Mathematical Science Laboratory of the Air Force Command and Control Development Division, Bedford, Massachusetts. The unit, containing 654 multiaperture devices (MADs), was built to prove the feasibility of interconnecting large numbers of magnetic elements in logical arrays. A single basic logic module built around two of the MAD elements was used throughout the unit. The module is a two-input OR gate with a positive or negative fan-out of three. Any one or more of the three outputs may be negative allowing combinations of OR and NOR logic in the same module. The unit will perform the operations of addition, subtraction, and multiplication on decimal numbers entered from a desk calculator type keyboard, with read out provided by incandescent indicators driven directly from the magnetic elements. Logic is included for up to ten digits, however registers have been presently constructed for only three digits.

Drive current for the unit is provided by a laboratory pulse generator and a current amplitude range of better than plus/minus ten percent has been achieved. Results indicate that with minor changes, larger all magnetic systems using MADs are entirely feasible.

**MISCELLANEOUS**

**CONTRIBUTIONS FOR DIGITAL COMPUTER NEWSLETTER**

The Office of Naval Research welcomes contributions to the NEWSLETTER. Your contributions will assist in improving the contents of this newsletter, and in making it an even better medium of exchange of information, between government laboratories, academic institutions, and industry. It is hoped that the readers will participate to an even greater extent than in the past in transmitting technical material and suggestions to this Office for future issues. Because of limited time and personnel, it is often impossible for the editor to acknowledge individually all material which has been sent to this Office for publication.

The NEWSLETTER is published four times a year on the first of January, April, July, and October, and material should be in the hands of the editor at least one month before the publication date in order to be included in that issue.

The NEWSLETTER is circulated to all interested military and government agencies, and the contractors of the Federal Government. In addition, it is being reprinted in the Communications of the Association for Computing Machinery.

Communications should be addressed to:

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Digital Computer Newsletter  
Information Systems Branch  
Office of Naval Research  
Washington 25, D. C.**

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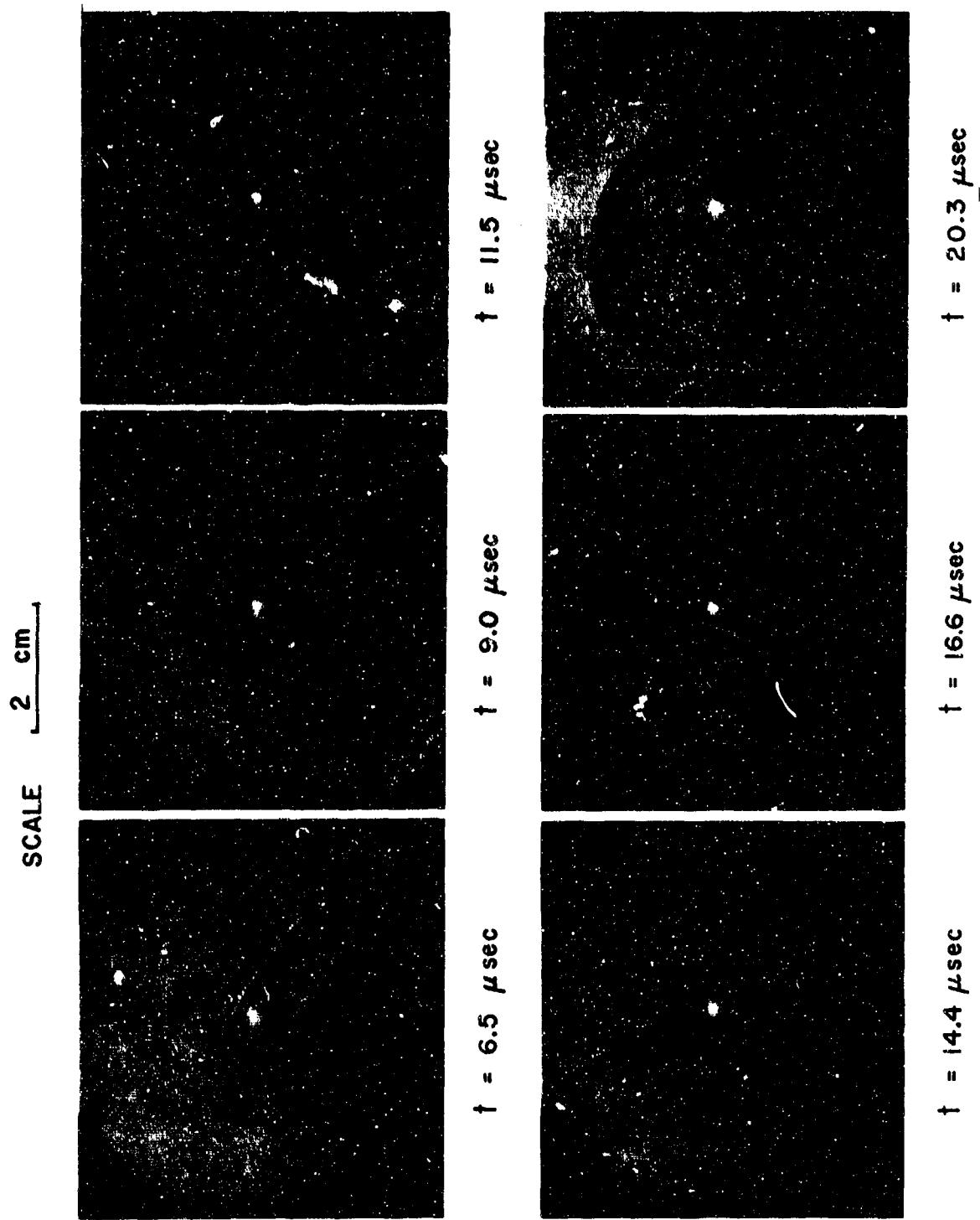


FIG. 14 SEQUENCE OF SPARK SCHLIEREN PHOTOGRAPHS ILLUSTRATING THE SPHERICAL DETONATION WAVE IN THE CRITICAL INITIATION ENERGY REGIME (MIXTURE: STOICHIOMETRIC OXY-ACETYLENE,  $P_0 = 100 \text{ mm Hg}$ ,  $E_0 = .3 \text{ JOULES}$ )